In force as of 15 September 2024

National control list

The general notes, acronyms and abbreviations, and definitions in the Part I of Annex I to the Dual-use Regulation (EU) 2021/821 are applicable on this annex.

Grouping and numbering of controls in this annex follows the form of the Annex I to the Dual-use Regulation (EU) 2021/821.

Section 1

Category 0: Nuclear materials, facilities and equipment

None.

Section 2

Category 1: Special materials and related equipment

None.

Section 3

Category 2: Materials processing

2A Systems, equipment and components

None.

2B Test, inspection and production equipment

2B901 Following additive manufacturing equipment, designed to produce metal or metal alloy components, having all of the following, and specially designed components therefor:

a. having at least one of the following consolidation sources:
   1. ”Lasers”;
   2. Electron beam; or
   3. Electric arc; and

b. having a controlled process atmosphere of any of the following:
   1. Inert gas; or
   2. Vacuum (equal to or less than 100 Pa); and

c. having any of the following 'in-process monitoring' equipment in a 'co-axial configuration' or 'paraxial configuration':
   1. Imaging camera with a peak response in the wavelength range exceeding 380 nm but not exceeding 14,000 nm;
   2. Pyrometer designed to measure temperatures greater than 1,273.15 K (1,000°C); or
   3. Radiometer or spectrometer with a peak response in the wavelength range exceeding 380 nm but not exceeding 3,000 nm; and

d. A closed loop control system designed to modify the consolidation source parameters, build path, or equipment settings during the build cycle in response to feedback from 'in-process monitoring' equipment specified in 2B901.c.

Technical Notes for the purposes of 2B901:

1. 'In-process monitoring', also known as in-situ process monitoring, pertains to the observation and measurement of the additive manufacturing process including electromagnetic or thermal emissions from the melt pool.

2. 'Co-axial configuration', also known as on-axis or inline configuration, pertains to one or more sensors that are mounted in an optical path shared by the 'laser' consolidation source.

3. 'Paraxial configuration' pertains to one or more sensors that are physically mounted onto or integrated into the 'laser', electron beam or electric arc consolidation source component.

4. For both 'co-axial configuration' and 'paraxial configuration', the field of view of the sensor(s) is fixed to the moving reference frame of the consolidation source and moves in the same scan trajectories of the consolidation source throughout the build process.

2C Materials

None.

2D Software

None.

2E Technology

2E901 "Technology" according to the General Technology Note for the "development" of equipment specified in 2B.

2E902 "Technology" according to the General Technology Note for the "production" of equipment specified in 2B.

2E903 "Technology", not specified elsewhere, for the "development" or "production" of 'coating systems' having all of the following:

a. Designed to protect ceramic "matrix" "composite" materials specified in 1C007 in Annex I to the Regulation (EU) 2021/821 from corrosion; and
b. Designed to operate at temperatures exceeding 1,373.15 K (1,100°C).

Technical Notes for the purposes of 2E903: 'Coating systems' consist of one or more layers (e.g., bond, interlayer, top coat) of material deposited on the substrate.

Section 4

Category 3: Electronics

3A Systems, equipment and components

3A901 Following electronic items:

Note: Integrated circuits include the following types:
-"Monolithic integrated circuits";
-"Hybrid integrated circuits";
-"Multichip integrated circuits";
-"Film type integrated circuits", including silicon-on-sapphire integrated circuits;
-"Optical integrated circuits";
-"Three dimensional integrated circuits";
-"Monolithic Microwave Integrated Circuits" ("MMICs").

a. Complementary Metal Oxide Semiconductor (CMOS) integrated circuits, not controlled in 3A001.a.2. in Annex I to Regulation (EU) 2021/821, designed to operate at an ambient temperature equal to or less (better) than 4.5 K.

Technical note: for the purposes of 3A901.a, CMOS integrated circuits are also referred to as cryogenic CMOS or cryoCMOS integrated circuits.

b. Parametric signal amplifiers having all of the following:
1. Designed for operation at an ambient temperature below 1 K (-272.15ºC);
2. Designed for operation at any frequency from 2 GHz up to and including 15 GHz; and
3. A noise figure less (better) than 0.015 dB at any frequency from 2 GHz up to and including 15 GHz at 1 K (-272.15ºC).

Note: Parametric signal amplifiers include Travelling Wave Parametric Amplifiers (TWPAs).

Technical Note: parametric signal amplifiers may also be referred to as Quantum-Limited Amplifiers (QLAs).

c. Integrated circuits having an aggregate bidirectional transfer rate of 600 Gbyte/s or more over all inputs and outputs and to or from other integrated circuits, not including volatile memories, and having or being programmable to have any of the following:
1. One or more digital processor units executing machine instructions having a 'total processing performance' of 6000 or more;
2. One or more digital 'primitive computational units', excluding those units contributing to the execution of machine instructions specified in 3A901.c.1., having a 'total processing performance' of 6000 or more;
3. One or more analogue 'primitive computational units' having a 'total processing performance' of 6000 or more; or
4. Any combination of digital processor units and 'primitive computational units' on an integrated circuit whose 'total processing performance' across 3A901.c.1, 3A901.c.2 and 3A901.c.3 add up to 6000 or more.

Note: Integrated circuits specified in 3A901.c include Graphical Processor Units (GPUs), Tensor Processing Units (TPUs), neural processors, in-memory processors, vision processors, text processors, co-processors/accelerators, adaptive processors, Field Programmable Logic Devices (FPLDs) and Application-Specific Integrated Circuits (ASICs).

Note: For "digital computers" and "electronic assemblies" containing integrated circuits specified in 3A901.c, see 4A902.

Technical Notes for the purposes of 3A901.c:

1.'Total Processing Performance' ('TPP') is the bit length per operation multiplied by the processing performance measured in Tera Operations Per Second (TOPS) over all processor units on the integrated circuit. For example, the 'TPP' for an integrated circuit having two digital processor units that are each capable of 200 TOPS at 16 bits is 6400 (2 processors × 200 TOPS × 16 bits = 6400). In 3A901.c.3, the 'TPP' of each analogue 'primitive computational unit' is the processing performance expressed in TOPS multiplied by 8.

2. A 'primitive computational unit' is defined as containing zero or more modifiable weights, receiving one or more inputs, and producing one or more outputs. A computational unit is said to perform 2N-1 operations whenever an output is updated based on N inputs, where each modifiable weight contained in the processing element counts as an input. Each input, weight, and output might be an analogue signal level or a scalar digital value represented using one or more bits. Such units include:

- Artificial neurons
- Multiply accumulate (MAC) units
- Floating-Point Units (FPUs)
- Analogue multiplier units
- Processing units using memristors, spintronics, or magnonics
- Processing units using photonics or non-linear optics
- Processing units using analogue or multi-level non-volatile weights
- Processing units using multi-level or analogue memory
- Suorittimet, jotka käyttävät monitasoista muistia tai analogista muistia
- Multi-value or multi-level units
- Spiking units

3. Operations relevant to the calculation of TOPS include both scalar operations and the scalar constituents of composite operations such as vector operations, matrix operations, and tensor operations. Scalar operations include integer operations, floating-point operations (often measured by FLOPS), fixed-point operations, bit-manipulation operations and/or bitwise operations.

4. The rate of TOPS is the maximum value theoretically possible when all processing units are operating simultaneously. The rate of TOPS and aggregate bidirectional transfer rate is assumed to be the highest value the manufacturer claims in a manual or brochure for the chip.

5. The bit length of an operation is equal to the highest bit length of any input or output of that operation. Additionally, if the processor unit is designed for operations that achieve different bits × TOPS values, the highest bits × TOPS value shall be used.

6. For processing units that provide processing of both sparse and dense matrices, the TOPS values are the values for processing of dense matrices (e.g., without sparsity).

3A903 Cryogenic cooling systems and components, as follows:

a. Systems rated to provide a cooling power greater than or equal to 600 µW at or below a temperature of 0.1 K (-273.05°C) for a period of greater than 48 hours;
b. Two-stage pulse tube cryocoolers rated to maintain a temperature below 4 K (-269.15°C) and provide a cooling power greater than or equal to 1.5 W at or below a temperature of 4.2 K (-268.95°C).

3B Testing, inspection and production equipment

3B901 Following manufacturing equipment for semiconductor components or semiconductor materials, and specially designed parts and components therefor:

a. Equipment designed for dry etching, having any of the following:

1. Equipment designed or modified for isotropic dry etching, having a largest 'silicon germanium-to-silicon (SiGe:Si) etch selectivity' of greater than or equal to 100:1; or
2. Equipment designed or modified for anisotropic dry etching, having all of the following;

a. Radio Frequency (RF) power source(s) with at least one pulsed RF output;
b. One or more fast gas switching valve(s) with switching time less than 300 ms; and
c. Electrostatic chuck with 20 or more individually controllable variable temperature elements.

Note 1: 3B901.a includes etching by 'radicals', ions, sequential reactions or non-sequential reactions.

Note 2: 3B901.a.2 includes etching using RF pulse excited plasma, pulsed duty cycle excited plasma, pulsed voltage on electrodes modified plasma, cyclic injection and purging of gases combined with a plasma, plasma atomic layer etching or plasma quasi-atomic layer etching.

Technical Note 1: For the purposes of 3B901.a, 'silicon germanium-to-silicon (SiGe:Si) etch selectivity' is measured for a Ge concentration of greater than or equal to 30% (Si0.70Ge0.30).

Technical Note 2: For the purposes of 3B901.a, 'radical' is defined as an atom, molecule or ion that has an unpaired electron in an open electron shell configuration.

b. 'EUV' masks and 'EUV' reticles designed for integrated circuits, other than those specified in 3B001.g. in Annex I to "the dual-use Regulation", and having a mask 'substrate blank' specified in 3B001.j. in Annex I to "the dual-use Regulation".

Technical Note 1: 'Extreme Ultraviolet' ('EUV') refers to electromagnetic spectrum wavelengths greater than 5 nm and less than 124 nm.

Technical Note 2: For the purposes of 3B901.b masks or reticles with a mounted pellicle are considered masks and reticles.

3B902 Scanning Electron Microscope (SEM) equipment designed for imaging semiconductor devices or integrated circuits, having all of the following:

a. Stage placement accuracy less (better) than 30 nm;
b. Stage positioning measurement performed using laser interferometry;
c. Position calibration within a Field-Of-View (FOV) based on laser interferometer length-scale measurement;
d. Collection and storage of images having more than 2 x 108 pixels;
e. FOV overlap of less than 5% in vertical and horizontal directions,
f. Stitching overlap of FOV less than 50 nm; and
g. Accelerating voltage more than 21 kV.

Note 1: 3B902 includes SEM equipment designed for chip design recovery.

Note 2: 3B902 does not control SEM equipment designed to accept a Semiconductor Equipment and Materials International (SEMI) standard wafer carrier, such as a 200 mm or larger Front Opening Unified Pod (FOUP).

3B903 Cryogenic wafer probing equipment having all of the following:
1. Designed to test devices at temperatures less than or equal to 4.5 K (-268.65°C); and
2. Designed to accommodate wafer diameters greater than or equal to 100 mm.

3C Materials

3C901. Epitaxial materials consisting of a 'substrate' having at least one epitaxially grown layer of any of the following:

a. Silicon having an isotopic impurity less than 0.08% of silicon isotopes other than silicon-28 or silicon-30; or
b. Germanium having an isotopic impurity less than 0.08% of germanium isotopes other than germanium-70, germanium-72, germanium-74, or germanium-76.

3C902. Fluorides, hydrides, or chlorides of silicon or germanium, containing any of the following:

a. Silicon having an isotopic impurity less than 0.08% of silicon isotopes other than silicon-28 or silicon-30; or
b. Germanium having an isotopic impurity less than 0.08% of germanium isotopes other than germanium-70, germanium-72, germanium-74, or germanium-76.

3C903. Silicon, silicon oxides, germanium or germanium oxides, containing any of the following:

a. Silicon having an isotopic impurity less than 0.08% of silicon isotopes other than silicon-28 or silicon-30; or
b. Germanium having an isotopic impurity less than 0.08% of germanium isotopes other than germanium-70, germanium-72, germanium-74, or germanium-76.

Note: 3C903 includes 'substrates', lumps, ingots, boules and preforms.
3D Software
3D901 "Software" designed to extract "GDSII" or equivalent standard layout data and perform layer-to-layer alignment from SEM images, and generate multi-layer 'GDSII' data or the circuit netlist. *Note: "GDSII" standard ("Graphic Design System II") is a database file format for data exchange of integrated circuit or integrated circuit layout artwork.*
3D902" Software" specially designed for the "use" of equipment specified in 3B901.a.
3D903 "Software" specially designed for the "development" or "use" of equipment specified in 3A901.b or 3B.
3E Technology
Technical Note: "Process Design Kit" ("PDK") is a software tool provided by a semiconductor manufacturer to ensure that the required design practices and rules are taken into account in order to successfully produce a specific integrated circuit design in a specific semiconductor process, in accordance with technological and manufacturing constraints (each semiconductor manufacturing process has its particular "PDK").
3E901 "Technology" according to the General Technology Note for the "development" and "production" of equipment and materials specified in 3A, 3B or 3C. Note: 3E901 does not control 'Process Design Kits' ('PDK') unless they include files that execute tasks or technology for equipment specified in 3A901.
3E902 "Technology" according to the General Technology Note for the "development" or "production" of integrated circuits or devices, using gate all-around field-effect transistors (GAAFET) structures. *Note 1: 3E902 includes 'process recipes'.* *Note 2: 3E902 does not control tool qualification or maintenance.* *Note 3: 3E902 does not control 'Process Design Kits' unless they include libraries that execute tasks or technology for equipment specified in 3A001 of Annex I of Dual-use Regulation (EU) 2021/821 or 3A901 of this annex.* *Technical Note: 'Process recipes' means a set of conditions and parameters for a particular process step.*
Section 5
Category 4: Computers

4A Systems, equipment and components

4A901 Quantum computers and related "electronic assemblies" and components therefor:

a. Following quantum computers:

1. Quantum computers supporting 34 or more, but fewer than 100, 'fully controlled', 'connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 10 -4;
2. Quantum computers supporting 100 or more, but fewer than 200, 'fully controlled', ' connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 10 -3;
3. Quantum computers supporting 200 or more, but fewer than 350, 'fully controlled', 'connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 2 x 10 -3;
4. Quantum computers supporting 350 or more, but fewer than 500, 'fully controlled', 'connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 3 x 10 -3;
5. Quantum computers supporting 500 or more, but fewer than 700, 'fully controlled', 'connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 4 x 10 -3;
6. Quantum computers supporting 700 or more, but fewer than 1,100, 'fully controlled', 'connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 5 x 10 -3;
7. Quantum computers supporting 1,100 or more, but fewer than 2,000, 'fully controlled', 'connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 6 x 10 -3;
8. Quantum computers supporting 2,000 or more 'fully controlled', 'connected' and 'working' 'physical qubits';

b. Qubit devices and qubit circuits, containing or supporting arrays of 'physical qubits', and specially designed for items specified in 4A901.a;
c. Quantum control components and quantum measurement devices, specially designed for items specified in 4A901.a.

Note 1: 4A901 includes circuit model (or gate-based) and one-way (or measurement-based) quantum computers. 4A901 does not control adiabatic (or annealing) quantum computers.

Note 2: Items specified in 4A901 may not necessarily physically contain any qubits. For example, quantum computers based on photonic schemes do not permanently contain a physical item that can be identified as a qubit. Instead, the photonic qubits are generated while the computer is operating and then later discarded.

Note 3: Items specified in 4A901.b are the following: semiconductor, superconducting, and photonic qubit chips and chip arrays; surface ion trap arrays; other qubit confinement technologies; and coherent interconnects between such items.

Note 4: 4A901.c includes items designed for calibrating, initialising, manipulating or measuring the resident qubits of a quantum computer.

Technical Notes for the purposes of 4A901: *1. A 'physical qubit' is a two-level quantum system used to represent the elementary unit of quantum logic by means of manipulations and measurements that are not error corrected. 'Physical qubits' are distinguished from logical qubits, in that logical qubits are error-corrected qubits comprised of many 'physical qubits'.* *2. 'Fully controlled' means the 'physical qubit' can be calibrated, initialised, gated, and read out, as necessary.* *3. 'Connected' means that two-qubit gate operations can be performed between any arbitrary pair of the available 'working' 'physical qubits'. This does not necessarily entail all-to-all connectivity.* *4. 'Working' means that the 'physical qubit' performs universal quantum computational work according to the system specifications for qubit operational fidelity.* *5. Supporting 34 or more 'fully controlled', 'connected', 'working' 'physical qubits' refers to the capability of a quantum computer to confine, control, measure and process the quantum information embodied in 34 or more 'physical qubits'.* *6. 'C-NOT error' is the average physical gate error for the nearest-neighbour two-'physical qubit' Controlled-NOT (C-NOT) gates.*
4A902 Computers, "electronic assemblies" and components containing one or more integrated circuits specified in 3A901.c. *Technical Note: In 4A902 computers include "digital computers", hybrid computers, and analogue computers.*
4B Test, inspection and production equipment
None.
4C Materials
None.
4D Software
4D901. "Software" specially designed or modified for the "development" or "production" of equipment specified in 4A901.b or 4A901.c.
4E Technology
4E901. "Technology" according to the General Technology Note for the "development" or "production" of equipment specified in 4A901.b, 4A901.c or 4D901.
4E902 "Technology" according to the General Technology Note for the "development", "production" or "use" of equipment or "software" specified in 4A902.

Section 6
Category 5: Telecommunications and ”information security”
None.
Section 7
Category 6: Sensors and lasers
None.
Section 8
Category 7: Navigation and avionics
None.
Section 9
Category 8: Marine
None.
Section 10
Category 9: Aerospace and propulsion
None.